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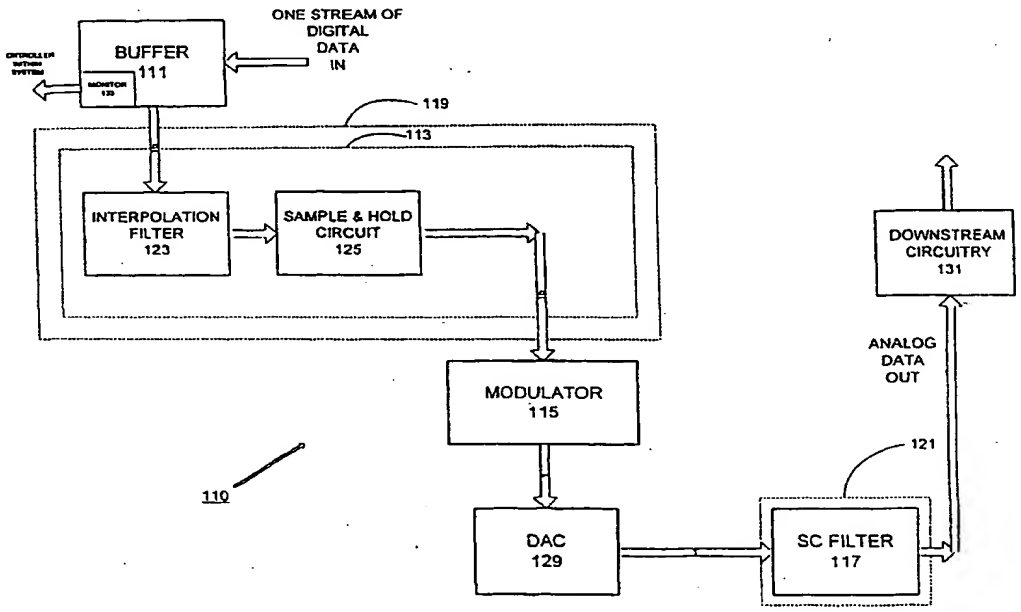

(57) Abstract

The invention dynamically compensates for differences in data rates for multistreamed systems, as shown in the figure. Any or all of the streams in a multistreamed system may be individually compensated at one time. In one embodiment, the status of an input buffer (111) for overflow or underflow is monitored (133) and used to change the number of oversamples (125) within a frame of one of the number of streams (16). An interpolation filter (123) is used for the generation of oversamples.

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VARIABLE CODEC FRAME LENGTH FOR MULTISTREAM APPLICATIONS

TECHNICAL FIELD

This invention relates to compensating data rates in multistream applications, and more particularly to modifying asynchronous data rates to compensate for data rate differences, within each stream, in successive blocks of a circuit.

BACKGROUND AND SUMMARY OF THE INVENTION

Data sent to a codec may be sourced at an asynchronous rate. Overflow or underflow of the data may result if the data rate in one portion of a circuit is different from the data rate in a following section.

For example, audio data sent via a streaming pipe over the internet may be played as it is downloaded, e.g., using an MPEG standard, such as MP3. Downloading starts, a buffer is accumulated, and then the data is decompressed and played while the remainder downloads. The rate at which the data may be received from the internet server is directly dependent on the type of modem connection and how variable that connection is over time. As time goes on, a poor connection may lead to, for example, loss of data packets. As packets are retransmitted, the host side buffer may be drained and the data may run out.

This possible problem is described in the context of a digital-to-analog converter ("DAC") system 10. A DAC system 10 includes a digital portion 19 and an analog portion 21. If the DAC is an oversampling delta-sigma type, the digital portion will typically include an interpolator 13. The interpolator 13 includes an interpolation filter 23 and a sample-and-hold circuit 25. The interpolation filter 23 increases the sample rate and removes or significantly attenuates energy at $f_s/2$ and above, where f_s is the input sampling frequency. The output of the interpolation filter 23 is processed through the sample-and-hold circuit 25 to provide an over-sampled output.

The output of the sample-and-hold circuit 25 is sent to modulator 15 which converts the oversampled signal into a one-bit data stream. The modulator 15 may be a delta-sigma modulator which provides good low level performance and can act as a one-bit digital quantizer. The one-bit data stream is sent to a one-bit DAC 29. The signal from the one-bit DAC 29 is then fed to the analog portion 21.

The analog portion 21 includes at least a filter 17. The filter 17 may be an analog low pass filter such as a switched capacitor filter.

A typical rate at which data may stream through the DAC system 10 may be 48 kHz. If this data is then passed to a downstream circuit which operates at a different speed, such as a constrained pipe, the data will either back up (if the downstream circuit operates at a lower speed), or stall (if the downstream circuit operates at a higher speed). For example, data may be recorded at 48 kHz and subsequently stored. The data may then be streamed to a system

through a constrained pipe at an average rate of 46 kHz. The output will periodically stall because the data rate through the constrained pipe cannot be increased.

A multistream system may include a plurality of such streams. Fig. 2 shows one embodiment of such a multistream system. In this system, a plurality of DACs 10A-10N may be employed, each attending to and servicing a stream A-N of an input multistream XX of data.

The present invention addresses the above problems on a stream-by-stream basis by dynamically compensating for differences in data rates. In one embodiment, the status of an input buffer of a stream is monitored and used to change the number of oversamples within a frame. In another embodiment, the input buffer of a stream is still monitored but a high frequency clock in the system is used to stall the codec for one clock. In both embodiments, distortion due to differences in data rates is reduced.

In one embodiment, the method includes steps of receiving samples of a signal of a stream at a sampling rate, oversampling the sampled signal to generate a prespecified number of oversamples per a frame, and deleting or repeating one or more of the oversamples per frame to remove the overflow or underflow condition.

In another embodiment, the method includes receiving samples of a signal of a stream at a sampling rate and oversampling the sampled signal to generate one of a prespecified number of oversamples per a frame. The prespecified number is equal to a nominal number in the absence of an overflow or underflow condition, the prespecified number is greater than

the nominal number in an underflow condition, and the prespecified number is less than the nominal number in an overflow condition.

In another embodiment, the method includes steps of receiving samples of a signal of a stream at a sampling rate, oversampling the sampled signal to generate a prespecified number of oversamples per a frame; and stalling the circuit for a number of cycles of the master clock to remove the overflow or underflow condition.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic block diagram of a prior art DAC system.

FIG. 2 is a schematic block diagram of a prior art multistreamed DAC system.

FIG. 3 is a schematic block diagram of a multistreamed DAC system according to an embodiment of the present invention.

FIG. 4 is a schematic block diagram of a multistreamed DAC system according to another embodiment of the present invention.

FIG. 5 is a schematic block diagram of a DAC system according to an embodiment of the present invention showing control of an input buffer for a single stream of data.

FIG. 6 is a schematic block diagram of a DAC system according to an embodiment of the present invention showing control of an input buffer via a variable interpolation filter for a single stream of data.

FIG. 7 is a schematic block diagram of a DAC system according to an embodiment of the present invention showing control of an input buffer via an interpolation filter and a frame controller for a single stream of data.

FIG. 8 is a schematic block diagram of a DAC system according to an embodiment of the present invention showing control of a stall condition by using a master clock to stall the codec for a clock cycle for a single stream of data.

Fig. 9 is a flowchart for an adaptive control loop according to an embodiment of the present invention for a single stream of data.

Fig. 10 shows a flowchart for the detection of an appropriate peak frame in a single stream of data for use in inserting or removing oversamples at random rates.

Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

The present disclosure addresses many of the aforementioned problems by, in part, managing an input buffer to the codec using a variable frame adjuster. Fig. 3 shows a schematic block diagram of the invention. A multistream input 501 includes N data streams labeled A-N. Each data stream A-N is incident, in the digital regime, on a variable frame adjuster 503A-503N. The adjusted data streams are each incident on a DAC 505A-505N. The nature of the variable frame adjusters 503A-503N and DACs 505A-505N is discussed in more detail below. Here it is noted that in one embodiment a variable frame adjuster and a DAC are combined in a unitary circuit.

In another embodiment, shown in Fig. 4, the streams from each variable frame adjuster are mixed in a mixer 507. A single stream is emitted from mixer 507, which is then sent to a DAC 509 for conversion. It is noted in this context that the mixer 507 may operate synchronously with a clock of its own, operating on all streams as though their data were "pull" type data. It may also be noted in this embodiment that the multistream mixing may result in less underflow conditions, due to the presence of many streams being mixed.

The various methods by which the variable frame adjusters may operate on streams is now discussed.

Fig. 5 shows such a variable frame adjuster in the context of a DAC system 110. In DAC system 110, the variable frame adjuster is included in the interpolation filter 123. In this DAC system 110, digital data flows to an input buffer 111 in digital portion 119. The digital portion 119 includes an interpolator 113 having an interpolation filter 123 and a sample-and-hold circuit 125. The data flows to a modulator 115 and a one-bit DAC 129. At this point the analog data is coupled to the analog portion 121 which includes a filter 117. The analog data then may flow out of the DAC system 110 and into downstream circuitry 131.

The contents of the input buffer 111 may be tested in a monitor 133. The monitor 133 may check for underflow, overflow, near underflow, or near overflow conditions. The results of the testing may be used to control various parts of the DAC system 110, or various parts of a circuit in which the DAC system 110 is located, in accordance with the principles of the invention. In particular, the status of the contents of the input buffer 111 as tested by

monitor 133 can be used to make adjustments to other parts of the system in order to accommodate differing data rates. The way in which such adjustments are made are presented below as example embodiments of the invention.

The status of the input buffer 111 can indicate whether the downstream rate is greater than or less than the upstream rate. For example, if the input buffer 111 is full or nearly full, the downstream rate is likely to be less than the upstream rate. In other words, the data rate is too high to be accommodated by all downstream circuitry beginning at the digital portion 119. If the input buffer 111 is empty or nearly so, the downstream rate is likely greater than the upstream rate. In general, it is preferable to allow the input buffer 111 to operate without running empty.

Management of the input buffer 111 may include lengthening or shortening the sample frames to accommodate the different data rates. In a first embodiment, the codec frame length is varied. In other words, the number of oversamples within the frame is varied. In this embodiment and others, the invention will be described in the context of a DAC system. However, one skilled in the art will recognize other systems in which the invention may be employed. For example, the invention may be employed in the context of an ADC or other devices in which both push-data and pull-data are present, such as a television tuner card in a computer. Of course, even the tolerance of a standard crystal oscillator in a system leads to differences in data rates.

The following definitions are used herein. When information is available to a system for immediate access on-demand, it is categorized as "pull data". This on-demand data may

be from any type of storage medium that provides a feedback path for control. Examples of this type include HDD, CD, DVD, PC memory systems, and many others.

When information is transferred or broadcast without regard to its reception and no data flow control feedback, it is categorized as "push data". This data type will not slow, stop, or retransmit for the receiver; therefore, the receiver must keep pace. Examples of this type include television broadcast, radio broadcast, and internet multicast.

It is also noted that while 128 oversamples is used throughout this description, the actual number may vary with the application. A system with any number of oversamples may effectively use the method of the invention.

One way of constructing this embodiment is shown by a DAC 210 in Fig. 6. This embodiment involves the use of a variable interpolation filter 145. As noted above, the interpolation filter is in part responsible for increasing or decreasing the sample rate. The variable interpolation filter 145 can generate extra or fewer oversamples for the given frame. In most cases, one extra or one fewer would be appropriate. By performing this in accordance with the oversampling rate, the distortion is reduced as compared with performing this at the original sample rate before the interpolation filter.

The digital portion 119 affects the input buffer 111 by way of data overflowing in the input buffer 111 or by the input buffer 111 running empty. In other words, the digital portion affects the input buffer 111 by overflowing or stalling. In a different embodiment, the digital portion 119 may actually provide a signal to input buffer 111 or to a monitor 133 within the

input buffer 111. This signal would then provide an indication of the state of the data rate in the downstream circuitry 131 or even downstream of the downstream circuitry 131.

Preferably, the input buffer never completely overflows or stalls. The monitor detects when these conditions are more likely to occur and signals the digital portion 119 to alter its number of oversamples per frame. The monitor, in this fashion, provides signals identifying a "near overflow" or a "near stall" condition or a rate of change indicating that such is likely to occur.

Once a signal is received indicating that a near stall or overflow condition has occurred, the signal is sent to a controller 137 within the variable interpolation filter 145. This signal may be sent from the monitor 133 within buffer 111. Once received, the signal causes the variable interpolation filter 145 to alter the number of oversamples per frame. In other words, rather than having the interpolation filter provide a uniform number of additional oversamples per input sample, the variable interpolation filter 145 inserts or deletes oversamples as required to avoid the stall or overflow condition described above. For example, if variable interpolation filter 145 usually inserts 128 oversamples per each input sample, a near overflow condition may cause the variable interpolation filter to insert only 127. Conversely, if variable interpolation filter 145 usually inserts 128 oversamples per each input sample, a near stall condition may cause the variable interpolation filter to insert 129. An appropriate number of coefficients is chosen for the extra or fewer oversamples. Appropriate control over the number of oversamples created is provided by the controller

137. In other words, in the example above, instead of 128 coefficients being chosen, 127 or 129 coefficients would be chosen.

In a different embodiment, rather than having a variable interpolation filter generate more or less oversamples per input sample, the interpolation filter may generate a fixed number of oversamples per input sample. However, once oversampling is completed, a particular oversample may be deleted or repeated in order to switch to a 127/129 oversample frame if required by a near overflow or near stall condition. This embodiment is shown in Fig. 7. In this figure, a DAC 310 has an interpolation filter 143 with two stages: an oversampling portion 139 and a frame controller 141. The oversampling portion 139 provides the requisite number of oversamples per sample, e.g., 128. The frame controller 141 deletes or repeats an oversample according to the stall or overflow condition. The determination of when the frame controller 141 is required to edit the number of oversamples may be made by the input buffer monitor 133 or by some other source, and is carried out via a controller 147. Of course, the controller 147 and the frame controller 141 may be within the same or different blocks of the circuit.

The location within the frame of the oversample that is deleted or inserted may be chosen in a random manner to avoid the generation of unwanted tonal components. Such a method is described below. If tonal component generation is not a factor, the location of the oversample chosen may be arbitrary. For example, the first oversample or the last oversample may always be the oversample chosen.

In both of these embodiments, any error introduced by the removal or addition of oversamples is spread over all (approximately) 128 oversamples. In other words, errors occur to oversampled values rather than to raw input samples so as to preserve data integrity.

In yet another embodiment, as shown by Fig. 8, no extra or fewer oversamples are created, nor are a set number of oversamples subject to a repetition or deletion of any one oversample. In this embodiment, the codec is stalled for one or more clock cycles. This embodiment is applicable to those situations where the interpolation filter creates an additional oversample, rather than where the interpolation filter causes the deletion of an oversample or the creation of fewer than the nominal number of oversamples.

Fig. 8 shows a master clock 151 controlling the interpolation filter 149. The master clock 151 may, of course, also control various other aspects of the system. Moreover, the master clock 151 may be used to create other clocks whose rates are either the same or are based on the master clock 151. The presence and rates of these other clocks depend on the requirements of the system. In this embodiment, the clock with the highest rate, here denoted MCLK 151, may be used as the basis for the stall procedure.

The MCLK 151 may be caused to stall for one or more clock cycles or alternatively for one or more phases of the MCLK 151. In this way, the downstream circuitry 131 may be allowed time to process the overflow oversamples and thus remove the overflow condition. The resulting frames in the codec would be slipped.

This embodiment may produce less distortion than the sampling based embodiments above. For example, a typical master clock rate may be MCLK = 24.576 MHZ. Using a half-clock stall leads to:

$$\frac{(2)(24.576\ MHz)}{48\ kHz} = 1024 \rightarrow 20 \log 1024 = 60\ dB$$

In this example, the clock stall thus provides 60 dB less distortion than the sample-based solutions because the master clock has a much higher resolution than the sample rate. It should be noted in this embodiment that the bus interface would need to operate asynchronously such that the bus would not see the stall of the MCLK 151.

In these embodiments, the monitor 133 of input buffer 111 may be used to detect and correct overflows or underflows in several ways. For example, low and high thresholds may be set and used to trigger the change in the frame length as described above. The resulting change in data consumption rate causes the input buffer 111 to move back between the low and high thresholds and the oversamples per frame are reset to nominal. If the tested parameter is not reset (due, e.g., to a large mismatch in data rates) the frame length may be adjusted further to increase the rate of recovery.

In another modification, rather than have a preset number of oversamples per frame, monitor 133 may consider the number of oversamples per frame to be a variable which is usually at a steady-state value but which varies with overflows and underflows. In this method, termed herein the "loop offset mode", thresholds are still set at low and high points but the number of oversamples per frame no longer tends towards a fixed value. Rather, the number of oversamples per frame tends towards whatever value is required to reduce the overflow or underflow.

For example, if the tested parameter indicates an underflow (the low threshold is passed), the number of oversamples per frame may increase to 129 from 128). This reduced the underflow to be eliminated. Rather than move back to 128, the number of oversamples per frame stays at 129 until the buffer falls below the low threshold again or above the high threshold. The loop offset mode may be especially useful when the sourcing rate is significantly different from the playback rate.

The error difference provided by adjusting the samples at 128x oversampling are two orders of magnitude greater than error concealment performed at the sample rate, reducing distortion effects by over 40 dB (e.g., 20 log 128 = 42 dB). Of course, the codec internal frame should be fully independent of the audio input frame.

Fig. 9 shows a flowchart for an adaptive control loop used in the codec input buffer for a single stream of data, and in particular an operation of an adaptive error concealment codec. Thresholds are established for both overflow and underflow conditions for each stream in the multistreamed data. The first step in each stream is subsystem initialization

201. A decision 203 is then made as to whether the adaptive circuit is enabled. This decision ensures that the codec has a mode that is compatible with industry codecs. If the adaptive circuit is enabled, then a determination is made as to whether the "loop offset mode" is enabled (step 205). As mentioned above, the loop offset mode is particularly suitable when rates vary significantly in different portions of a system because the frame size may continue to be modified in a rate-adaptive manner. If the loop offset mode is enabled, then the determination of overflow (step 207) or underflow occurs (step 209). For example, if the input buffer falls below the low threshold (underflow step 209), each consecutive frame in which the buffer is below the low threshold has a frame length that is increased (step 211), e.g., by one oversample value. Once the playback rate matches the source rate, the buffer status moves back above the low threshold and stabilizes at a frame size appropriate for the incoming data. If an overflow condition occurred, each consecutive frame in which the buffer is above the high threshold has a frame length that is decreased (step 213), e.g., by one oversample value. In both the case of an underflow and where the number of oversamples per frame is decreased, a test for an empty buffer (step 215) may occur. In both underflows and overflows, the frame size is adjusted to compensate and the final size of the frame is calculated (step 219) from the loop responses. The net effect is that the data is played at a rate that is different from its recorded rate; however, empty frames do not occur, nor do overflows.

If the loop offset mode is not enabled, then the frame length is reset, for each frame, to the preset value (e.g., 128 oversamples per frame) (step 217). For small drifts between the source data and the playback, this way may be preferred and allows for instantaneous correction with low distortion. It should be noted that this flowchart is only representative of one of the several methods available.

It should also be noted that when oversample insertion or removal occurs at a periodic rate, there is a tonal component generated at the rate of insertion or removal. If the rate of insertion or removal is randomized, the tonal energy will be distributed over a wide range and the overall tonal component will be small enough to be unnoticeable.

In order to achieve a random insertion or removal rate, the timing in which the interpolator may be caused to insert or remove an oversample may be adjusted. In particular, when the interpolator receives a request for an oversample skip or repeat, the interpolator may simply insert or remove the oversample accordingly; however, this may lead to the tonal generation above. Instead, the interpolator may choose to wait to insert or remove the oversample until a prespecified time. The appropriate prespecified time to insert or remove an oversample may be when the frame's oversamples have an extremal value (i.e., a maximum or minimum at approximately zero slope). At these points, addition or removal of oversamples does not result in a significant change in the frequency components. A certain time period is added but little distortion is added.

One method of determining the extremal value is shown in Fig. 10. Fig. 10 shows an extremal detection flowchart. Initially, an extremal flag is reset (step 301). The first test may be for a negative slope of the current frame (step 303). If the slope is negative, then the following frame slope is tested (step 305). If this slope is not negative, then the extremal flag is set (step 307) and the insertion or removal may proceed. If this slope is negative, other sample processing may occur (step 309) and the slope detect procedure is begun again. If the current frame slope is not negative, then the following frame slope is tested (step 311). If this slope is negative, then the extremal flag is set (step 313) and the insertion or removal may proceed. If this slope is not negative, other sample processing may occur (step 309) and the slope detect procedure is begun again. Again, it is noted that this flowchart is only representative of one of the several methods available.

It should be noted that if no extreme is available after waiting a prespecified period of time, the interpolator may be forced to insert or remove the oversample despite the lack of an extremal frame (e.g., a 20 Hz input with extremes every 25 ms).

It is noted that the source data frame sync and the internal codec frame sync do not need to sync-up because each incoming stream is destined for the analog domain. Thus, in the context of the system which generated the incoming stream, there is no longer a frame of discrete reference. The data is in continuous time, allowing full decoupling of the data bus frame sync from the internal codec frame sync.

Example of Error Accumulation

The accumulated error, when an extra audio oversample is created (to account for data rate disparities in a system), may be estimated as follows. The master clock for audio may be operating at, e.g., 48 kHz x 128 x 2 = 12.288 MHZ. The oversampling rate is 48 kHz times the number of oversamples per frame (128) = 6.144 MHZ. With the oversample rate of 128, if the frame were lengthened to 129, the number of audio samples per second would be 48,000 x 128/129 = 47,628.

For typical oscillators, at a 50 PPM / clock accuracy, a 100 PPM error could result from the two clocks. At 48 kHz, this results in 4.8 samples per second drift between subsystems. At 1/10,000 of the distribution of 128 oversamples, this leads to 10,000/128 or 78. In other words, one extra or fewer oversamples would be generated each 78 audio samples.

A number of embodiments of the present invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, the invention may be utilized in a number of other codec-type devices besides DACs. As another example, in the embodiment of Fig. 4, some of the streams may be mixed in mixer 507 and others may be sent to individual DACs. Moreover, the invention is intended to encompass any sample rates, oversample rates, master clock rates, DAC bit resolution, etc. The values used here are only for illustrative purposes and should not be considered limiting. Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A multistreamed circuit with variable frame adjustment per stream, comprising:

a source of multistreamed data, said multistreamed data including a plurality of streams of data; a plurality of variable frame adjusters coupled to said plurality of streams of data, each of said frame adjusters to alter the number of oversamples in each stream of data upon the occurrence of a control signal assertion.

2. The circuit of claim 1, where the control signal assertion is generated by an occurrence of a condition selected from the group consisting of an underflow, an overflow, a near-underflow, or a near-overflow.

3. The circuit of claim 1, further comprising a plurality of data converters coupled to said plurality of variable frame adjusters.

4. The circuit of claim 1, wherein one of said plurality of data converters is a digital-to-analog converter.

5. The circuit of claim 1, further comprising a mixer coupled to said plurality of variable frame adjusters.

6. The circuit of claim 5, further comprising a data converter coupled to said mixer.

7. The circuit of claim 6, wherein said data converter is a digital-to-analog converter.

8. The circuit of claim 2, wherein each of said plurality of variable frame adjusters includes: an interpolation filter to generate a fixed number of oversamples for an input sample; a frame controller coupled to the interpolation filter to delete or repeat at least one of the number of oversamples generated; a buffer for holding the input sample prior to the generation of oversamples; and a monitor to test the buffer, the monitor coupled to the frame controller to provide the frame controller with an overflow, near-overflow, near-underflow, or underflow condition in a circuit.

9. The circuit of claim 2, wherein each of said plurality of variable frame adjusters includes: a variable interpolation filter to generate oversamples for an input sample within the multistream; a controller coupled to the variable interpolation filter to control the number of oversamples generated; a buffer for holding the input sample prior to the generation of oversamples; and a monitor to test the buffer, the monitor coupled to the controller to provide the controller with an overflow, near-overflow, near-underflow, or underflow condition in a circuit.

10. The circuit of claim 2, wherein each of said plurality of variable frame adjusters includes: an interpolation filter to generate a number of oversamples for an input sample; a master clock coupled to the interpolation filter to control the operation of the interpolation filter; a buffer to hold the input sample prior to the generation of oversamples; and a monitor to test the buffer for an underflow or near-underflow condition, the monitor coupled to the master clock to stall the master clock upon the occurrence of an underflow or near-underflow condition to at least partially compensate for an underflow or near-underflow condition.

11. A method of dynamically compensating for an overflow or underflow condition in a multistreamed circuit, comprising: sampling a multistreamed signal at a sampling rate to generate a plurality of sampled streams of data; oversampling each sampled signal to generate a prespecified number of oversamples per a frame; changing an amount of oversampling per frame to at least partially compensate for the overflow, near-overflow, near-underflow, or underflow condition.

12. The method of claim 11, further comprising detecting the overflow, near-overflow, near-underflow, or underflow condition by testing the status of an input data buffer.

13. The method of claim 11, further comprising detecting the overflow, near-overflow, near-underflow, or underflow condition by testing the status of a data buffer in a portion of a downstream circuit.

14. The method of claim 11, further comprising generating a number of coefficients equal to the prespecified number.

15. A method of dynamically compensating for an overflow, near-overflow, near-underflow, or underflow condition in a multistreamed circuit, comprising: sampling a multistreamed signal at a sampling rate to generate a plurality of sampled streams of data; oversampling each sampled signal to generate one of a prespecified number of oversamples per a frame, the prespecified number equal to a nominal number in the absence of an overflow, near-overflow, near-underflow or underflow condition, the prespecified number greater than the nominal number in an underflow or near-underflow condition, and the prespecified number less than the nominal number in an overflow or near-overflow condition.

16. The method of claim 15, wherein the prespecified number is equal to the nominal number, or equal to the nominal number plus or minus one oversample.

17. The method of claim 15, further comprising detecting the overflow, near-overflow, near-underflow, or underflow condition by testing the status of an input data buffer.

18. The method of claim 15, further comprising detecting the overflow, near-overflow, near-underflow or underflow condition by testing the status of a data buffer in a portion of a downstream circuit.

19. The method of claim 15, further comprising generating a number of coefficients equal to the prespecified number.

20. A method of dynamically compensating for an underflow or near-underflow condition in a multistreamed circuit having a master clock, comprising: sampling a multistreamed signal at a sampling rate to generate a plurality of sampled streams of data; oversampling each sampled signal to generate a prespecified number of oversamples per a frame; and stalling a number of the plurality of sampled signals for a number of cycles of the master clock to remove the underflow or near-underflow condition.

21. The method of claim 20, further comprising detecting the underflow or near-underflow condition by testing the status of an input data buffer.

22. The method of claim 20, further comprising detecting the underflow or near-underflow condition by testing the status of a data buffer in a portion of a downstream circuit.

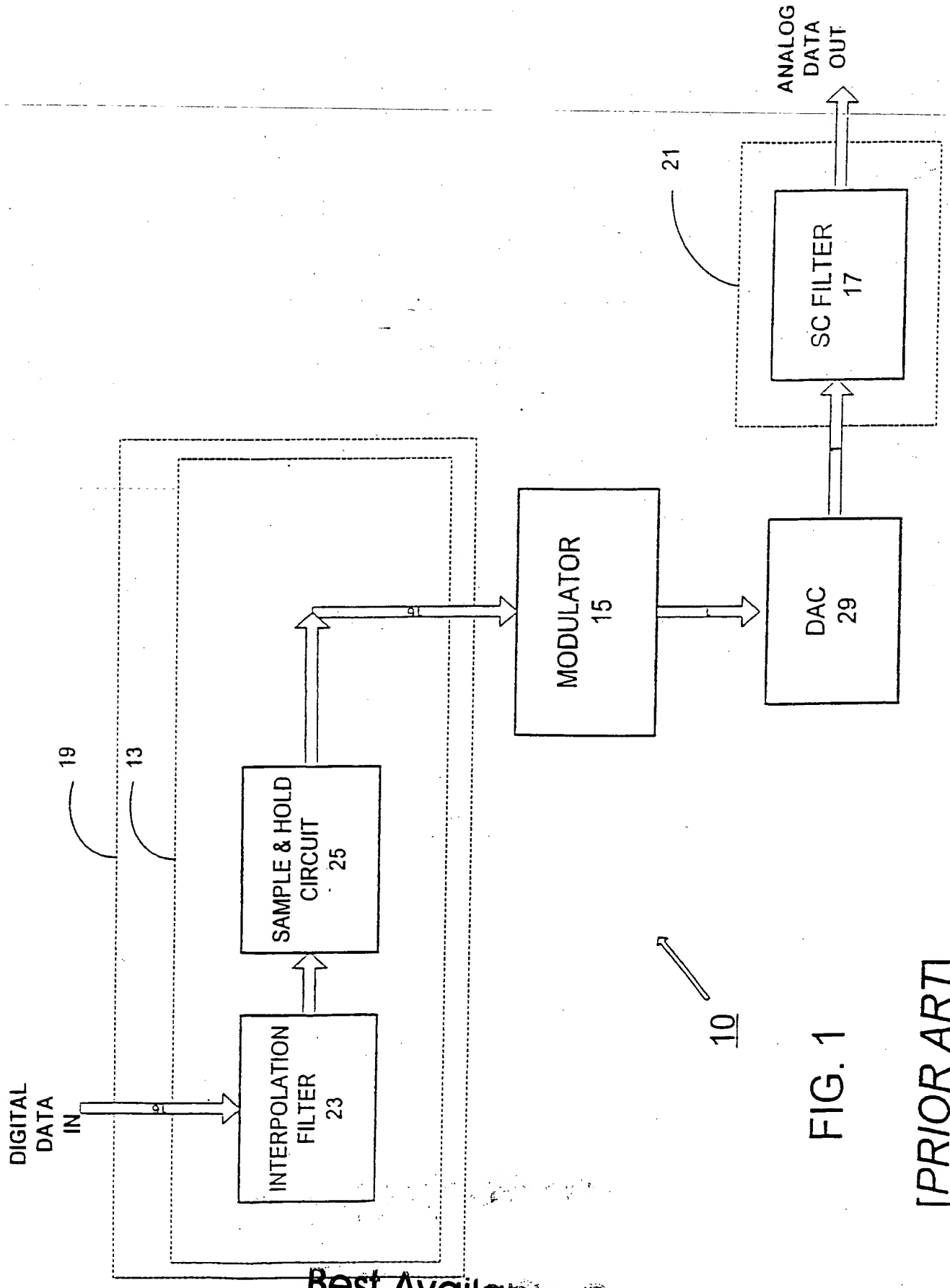

FIG. 1 [PRIOR ART]

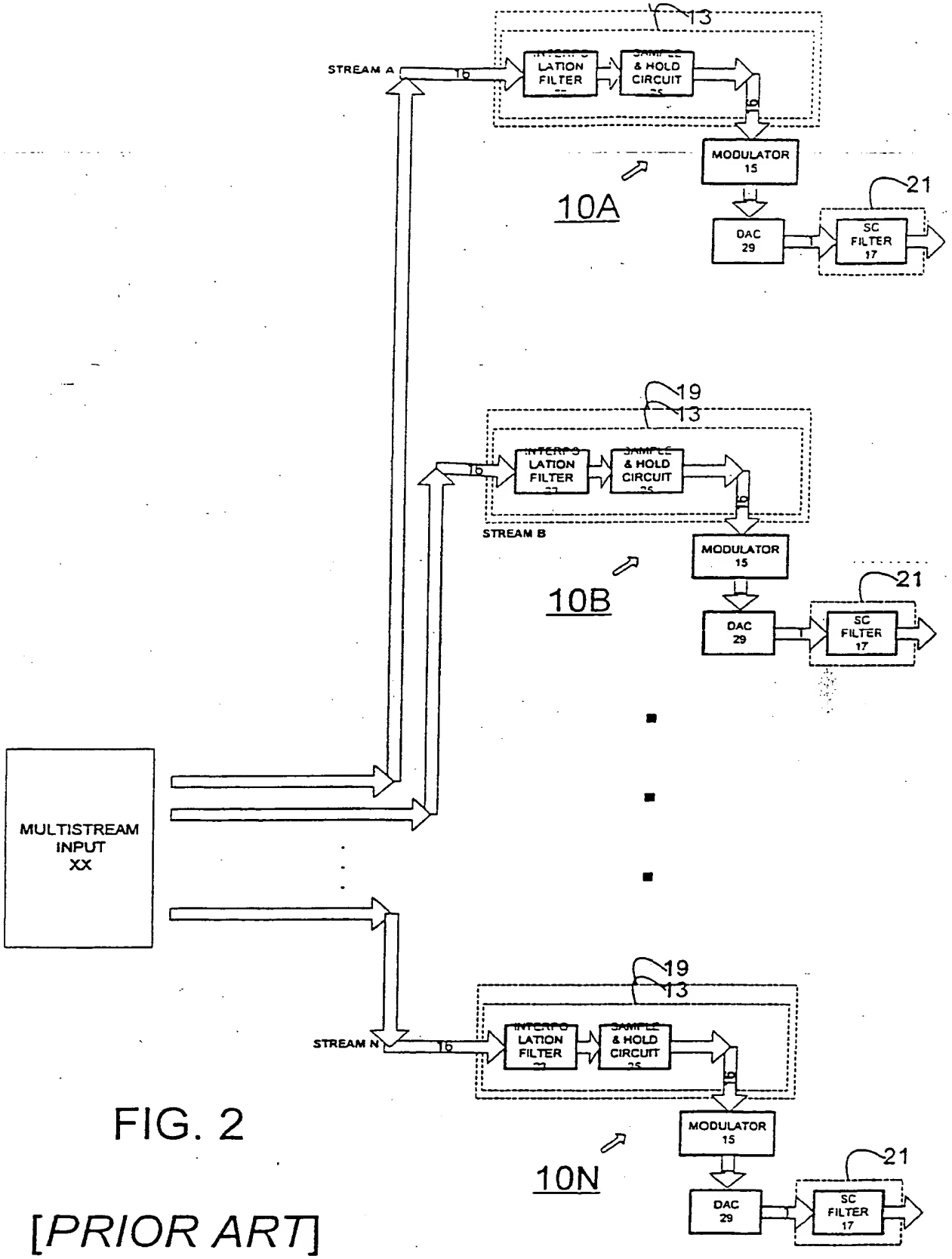

FIG. 2

[PRIOR ART]

Best Available Copy

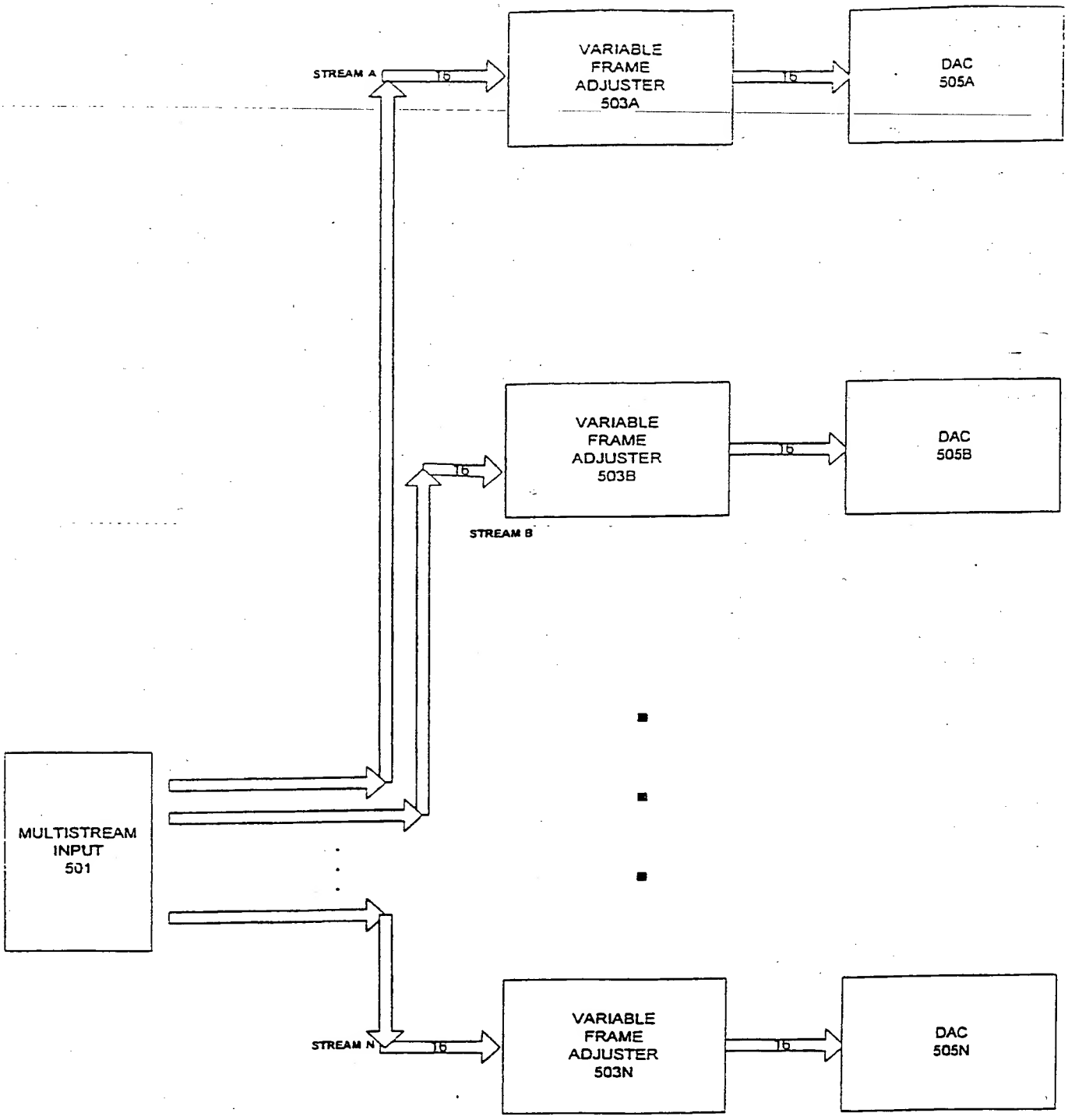

FIG. 3

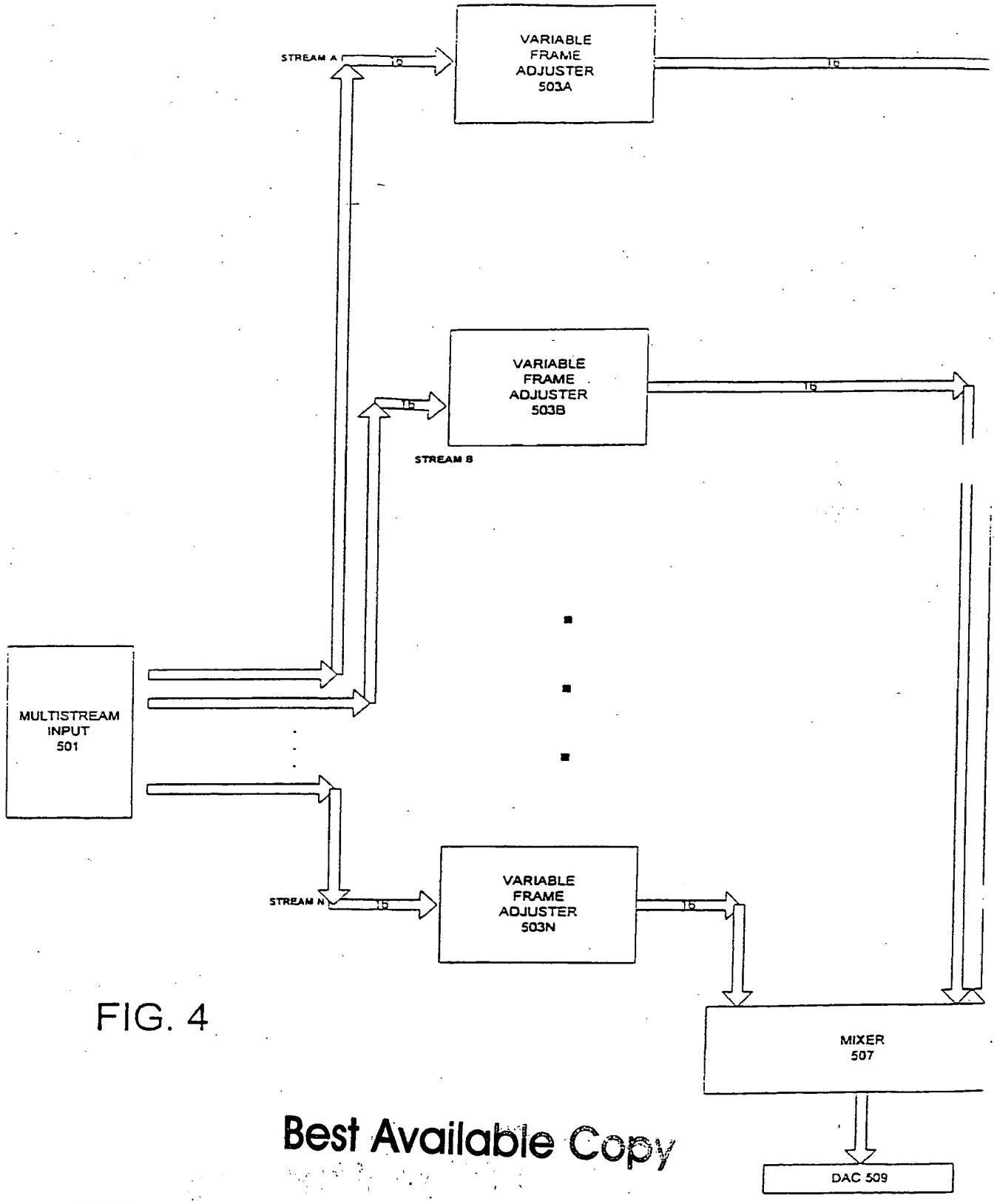

FIG. 4

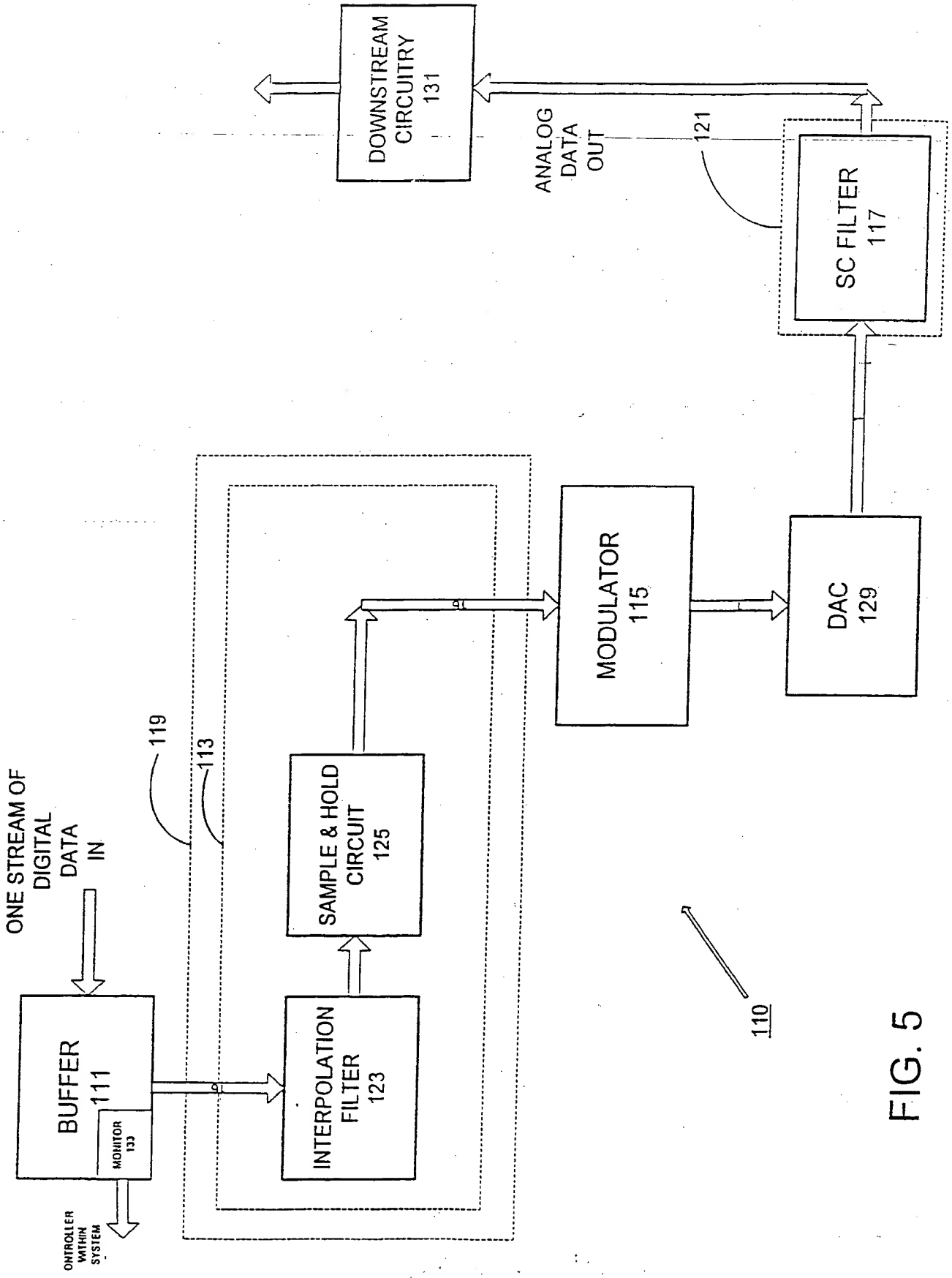

FIG. 5

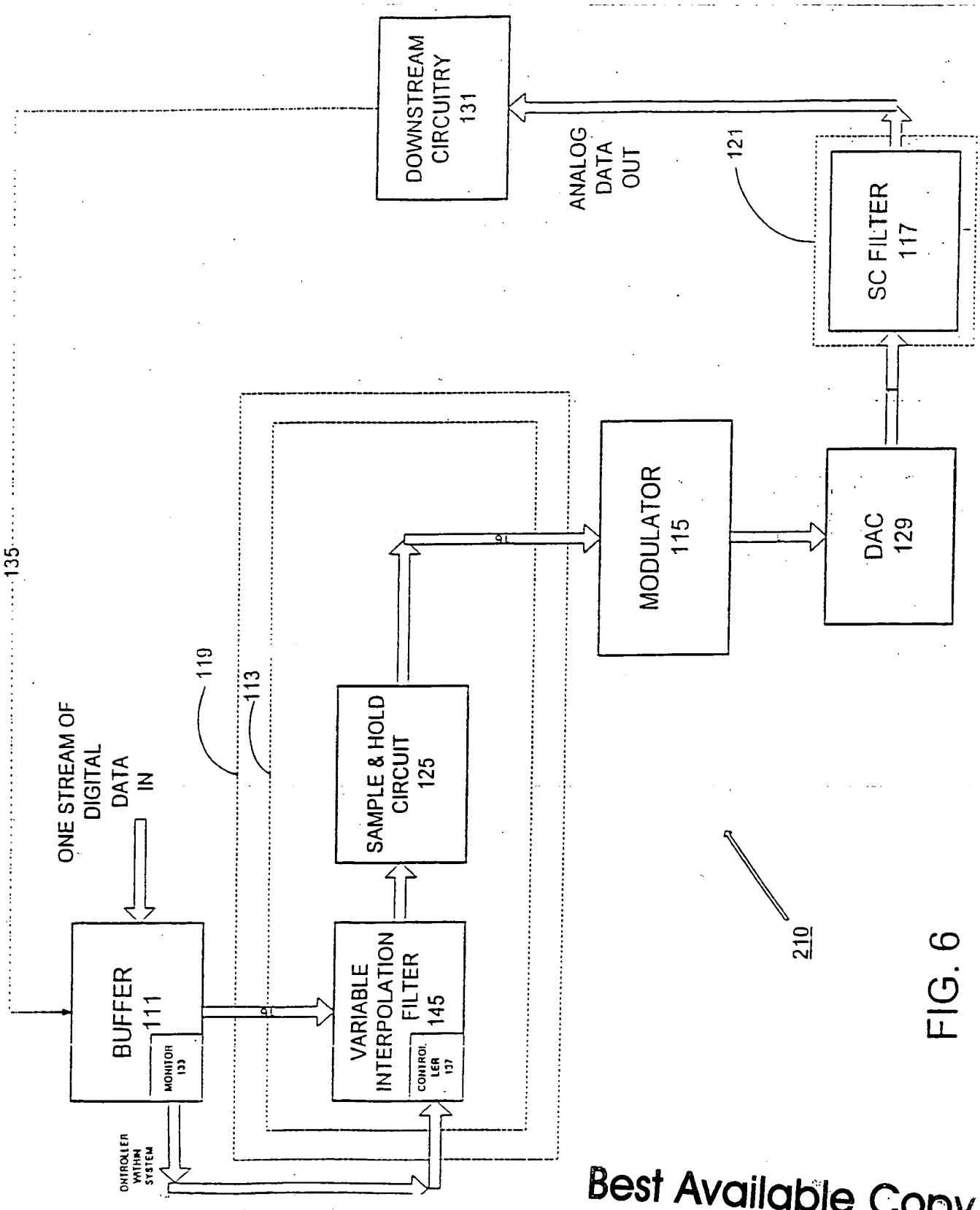

FIG. 6

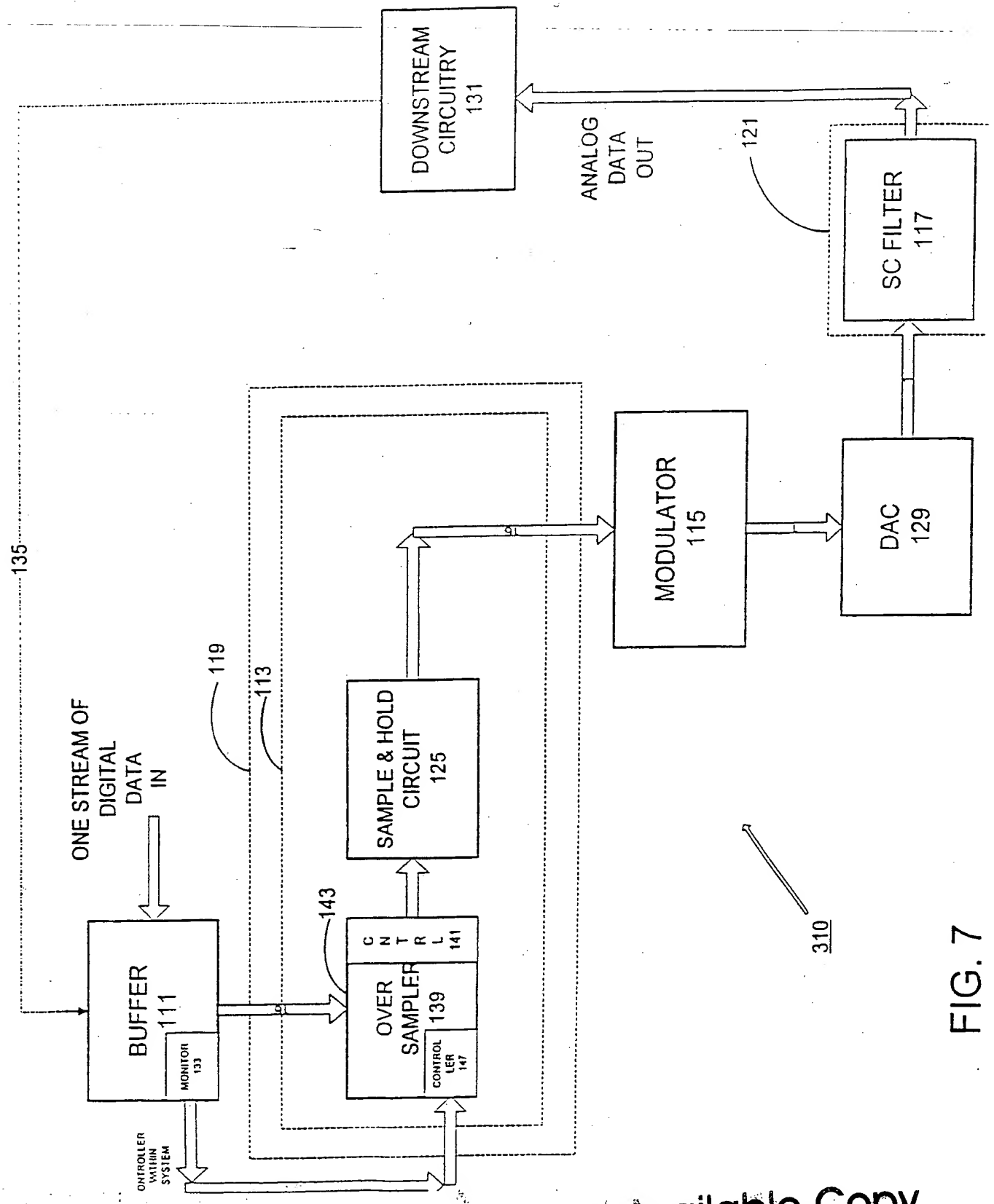

FIG. 7

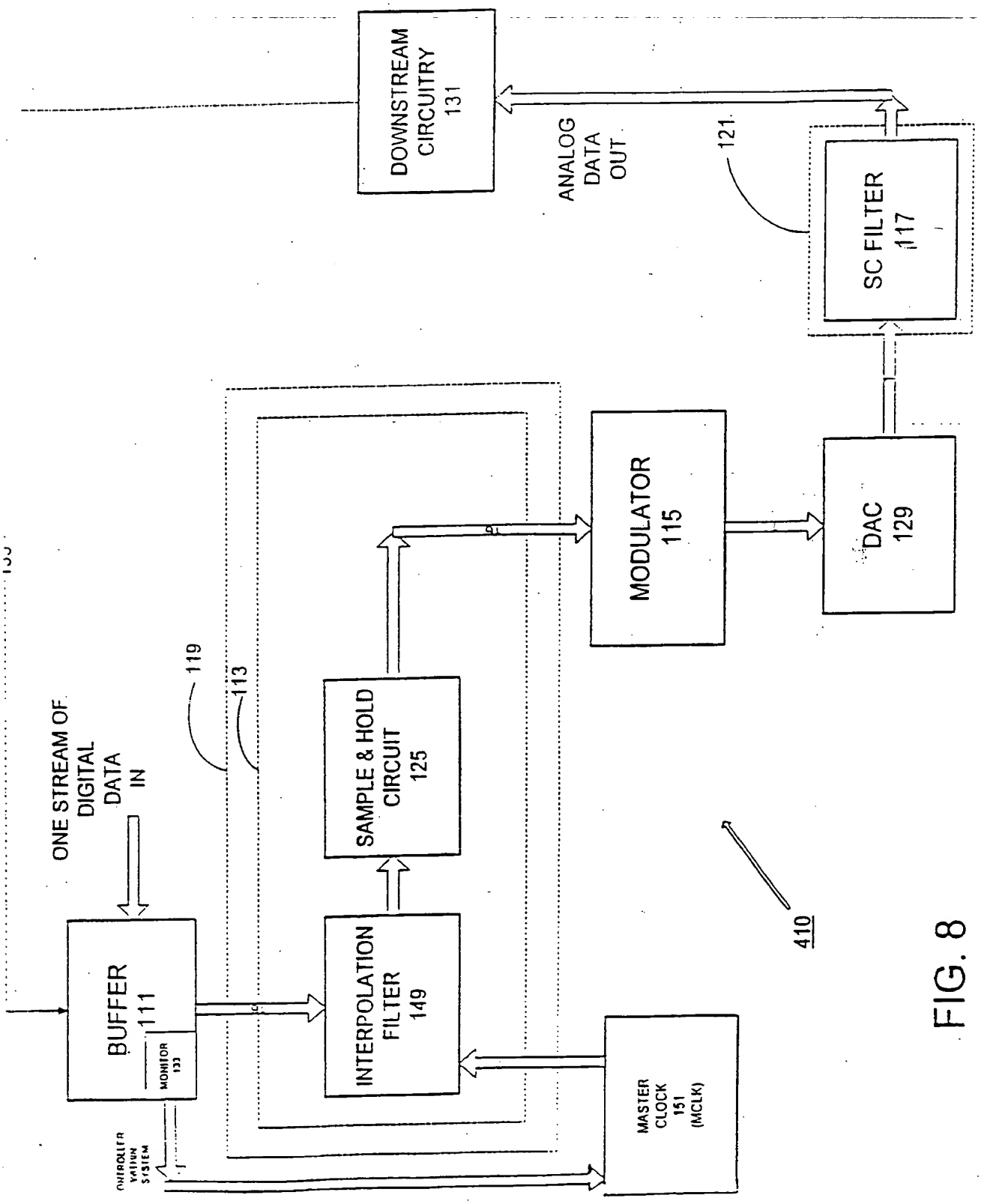

FIG. 8

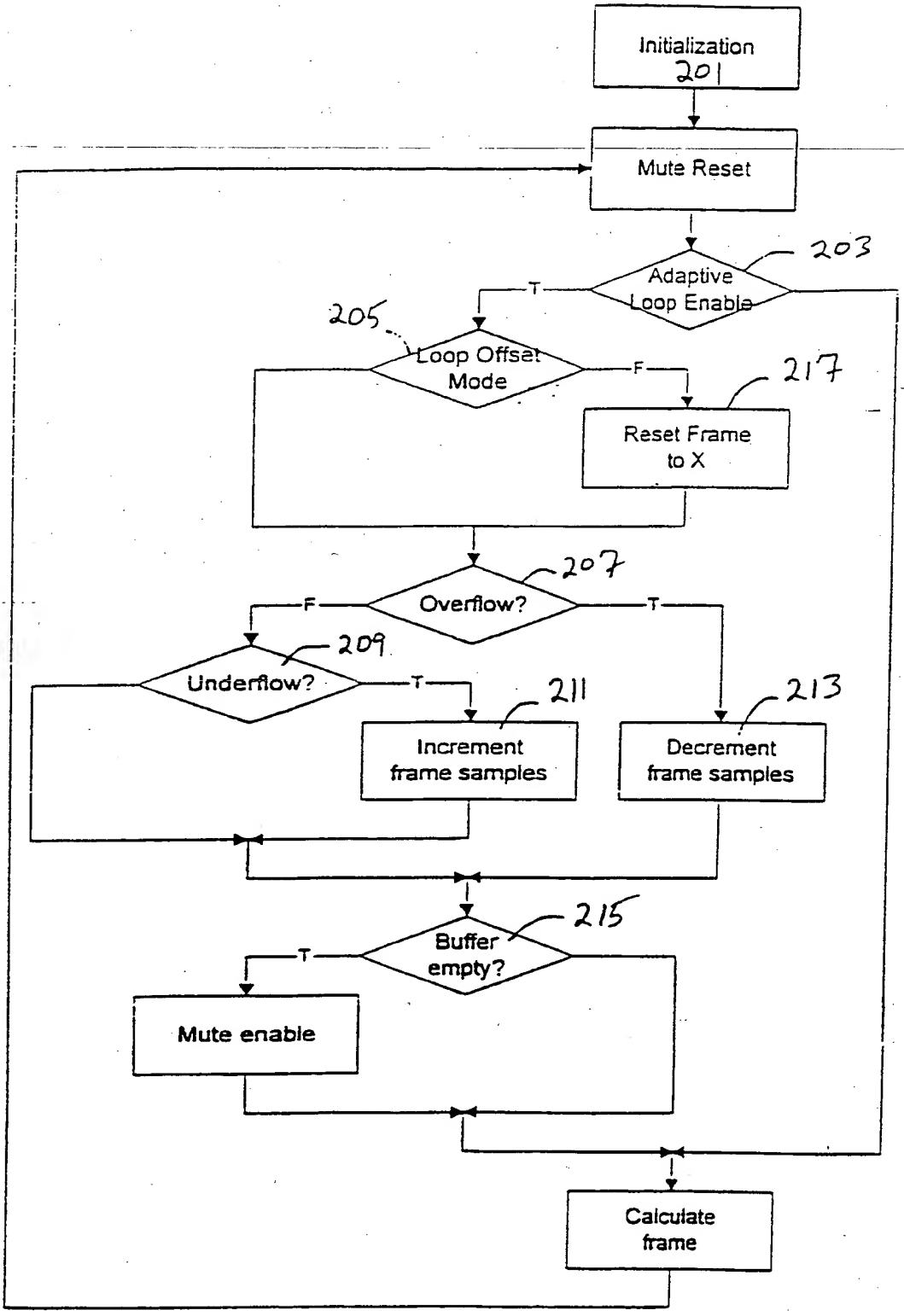

Fig. 9

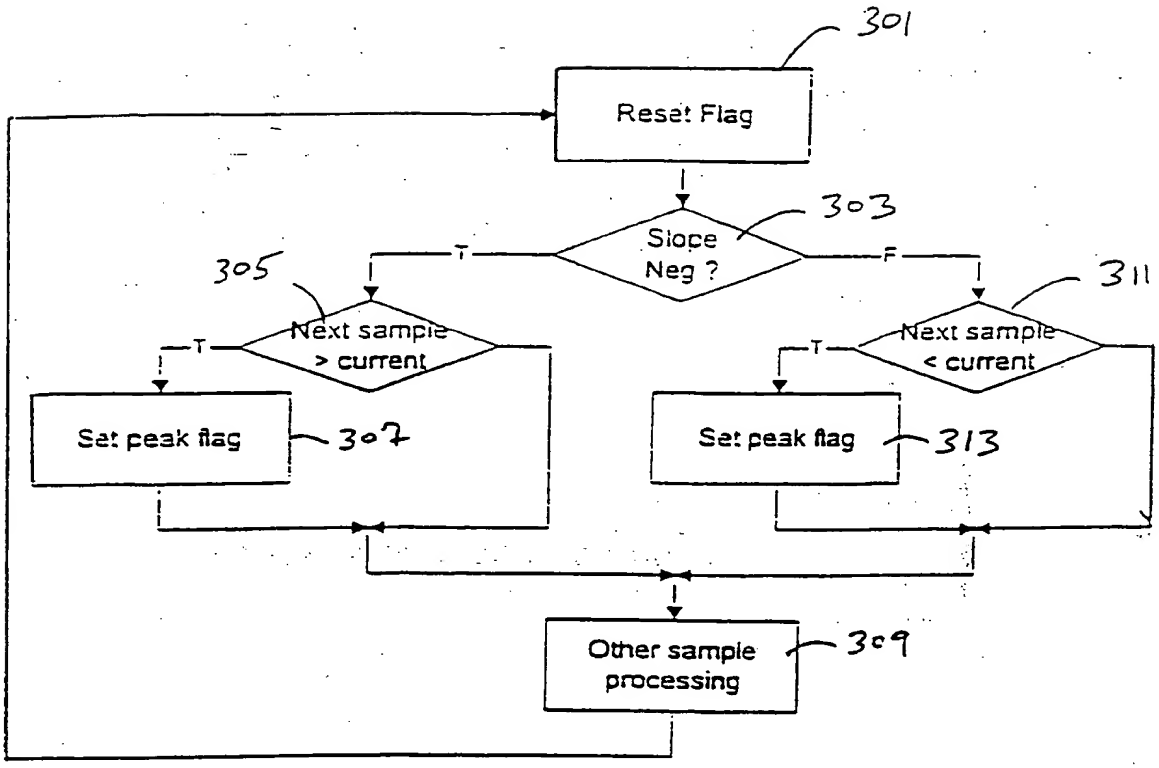

Fig. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/15408

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H04J 3/24; H04N 7/50
US CL :348/419; 370/468; 710/57
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 348/419,714-719; 370/465,468,470,471,472,473,229; 710/52-57

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS and WEST
Serach items: overflow, underflow, buffer, monitor?, decoder, receiver, and encoder

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,619,341 A (AUYEUNG et al.) 8 April 1997, Fig. 2 and col. 3, lines 50-67.	1-7,11-22
Y,P	US 5, 914,960 A (RAUHALA et al.) 22 June 1999, Fig. 1 and Abstract	1-8 and 11-22
Y	US 5,398,072 A (Auld) 14, March 1995, Fig. 2 and Fig. 3, Abstract	1-8 and 11-22
Y	US 5,663,962 A (Caire et al.) 2 Septeber 1997, Fig. 1A	1-22
Y,P	US 5,905,732 A (Fimoff et al.) 18 May, 1999, Fig. 4, col 3, lines 1-9.	1-8 and 11-22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier document published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 SEPTEMBER 1999	21 OCT 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer SEEMA S. RAO Telephone No. (703) 308-3900

Form PCT/ISA/210 (second sheet)(July 1992)★